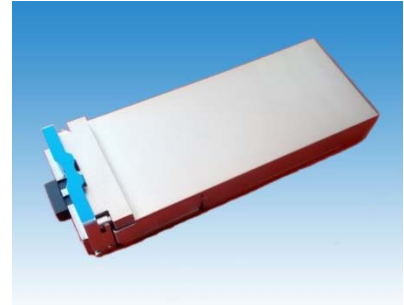


## 100G-BASE-LR4 10km CFP2 Optical Transceiver

SOCP2-LR4-10

### Features

- Hot Pluggable CFP2 MSA package
- IEEE 802.3ba 100GBASE-LR4 compliant
- CFP-MSA-CFP2-HW-Specification compliant
- Up to 10km for G.652 SMF
- Receiver: 4x 25Gb/s PINROSA
- Transmitter: 4x 25Gb/s WDM TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- 4x 28G Electrical Serial Interface (CEI-28G-VSR)
- MDIO management interface with Digital Diagnostic
- +3.3V power supply
- Power consumption less than 9W
- Compact size: 107.5 x 41.5 x 12.4 mm
- Operating case temperature: 0 to +70 °C
- Duplex LC Receptacle
- ROHS-6 compliant



### Applications

- 100G Base-LR4 Ethernet
- OTU4

### Description

SOCP2-LR4-10 transceivers are designed for use in 100Gigabit Ethernet link over 10km single module fiber, and it is compliant to the CFP MSA CFP2 HW Specification and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics are available via MDIO as specified in the CFP MSA Management Interface Specification.

The transceiver's design is optimized for high performance and cost efficiency to provide customers the best solutions for Data com and Telecom applications.

The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

### Product Selection

SO-100G-CFP2-LR4

TR: Transceiver  
4: 100Gb/s  
C21: CFP2 Solution 1L:  
10km

# 1 100Gb/sCFP2electricalparameters

## 1.1 AbsoluteMaximumRatings

The limit of the maximum value is shown as below Table 1. (If operating out the limit of the maximum value will cause permanent damage).

Table 1 100Gb/sCFP2 module limit the maximum value

Parameter	Symbol	Conditions	Min.	Max	Unit
Storage temperature (case)	T <sub>stg</sub>	—	-40	+85	°C
Relative humidity	RH	0	—	85	%
Damage Threshold for Receiver	P <sub>max</sub>	—	—	+10.0	dBm
Power Supply	V <sub>cc</sub> 3.3V	—	-0.3	+3.6	V
	V <sub>cc</sub> 5.0V	—	—	—	V
Input 3.3V LVCMOS signal level	V <sub>i</sub>	—	-0.3	V <sub>cc</sub> +0.3	V
Input 1.2V LVCMOS signal level	V <sub>i</sub>		-0.3	1.6	V
ESD Sensitivity on module and all host pins	HBM	Human Body model R=1.5K,	—	2000	V

## 1.2 Recommended operating conditions

The recommended working conditions are shown as below Table 2.

Table 2 100Gb/sCFP2 recommended working conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	T <sub>c</sub>	0	—	+70	°C
Supply voltage	V <sub>cc</sub> 3.3V	+3.14	+3.3	+3.47	V
Supply Current	I <sub>cc</sub> 3.3V	—	—	2.56	A
Power dissipation	P	—	—	9	W
Low Power dissipation	P <sub>Low</sub>			2	W
In-rush Current	I <sub>-inrush</sub>			200	mA/us
Turn-off rush Current	I <sub>-turnoff</sub>	-200			mA/us
Link Distance	L	2M	—	10km	G.652SMF

## 2 100Gb/s CFP2 Specifications

### 2.1 Optical Specifications

Table 3 100Gb/s CFP2 Optical Specifications (100GBase-LR4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter</b>						
Channel data rate				25.7812		Gbps
Aggregated data rate				103.125		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	$\lambda_{c0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{c1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{c2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{c3}$		1308.09	1309.14	1310.19	nm
Total Average Launch Power	P <sub>out</sub>		—	—	10.5	dBm
Average Launch Power per Lane	P <sub>each</sub>		-4.3	—	4.5	dBm
Average Launch Power of TX_DIST Transmitter per lane	P <sub>off</sub>	TX_DIST=H	—	—	-30	dBm
Extinction Ratio	E <sub>R</sub>		4	5.5	—	dB
SMSR	SMSR		30	—	—	dB
Dispersion Penalty	DP	10km SMF	—	—	2.2	dB
Relative Intensity Noise	RIN	Mod off	—	—	-130	dB/Hz
Optical Return Loss Tolerance	T <sub>RL</sub>		—	—	20	dB
Transmitter reflectance	T <sub>ef</sub>		—	—	-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3} <sup>1</sup>	EM		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
<b>Receiver</b>						
Channel data rate				25.7812		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	$\lambda_{r0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{r1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{r2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{r3}$		1308.09	1309.14	1310.19	nm

Damagethreshold	$P_{DT}$		—	5.5	—	dBm
Averagereceiverpowerper lane	Rpow		-10.6	—	4.5	dBm
ReceiverSensitivity(OMA)per lane	Psen		—	—	-8.6	dBm
StressedReceiverSensitivity per Lane	Psen_str		—	—	-6.8	dBm
Receiver Reflectance	Ref		—	—	-26	dB
Conditions ofstressed receiversensitivitytest						
Verticaleyeclosurepenalty per Lane			—	—	1.8	dB
Stressed eyejitter perLane			—	—	0.3	UI
Rx-LaneLOSAssert			—	-18	—	dBm
Rx-LaneLOSDeassert			—	-15	—	dBm
Rx-LaneLOSHysteresis			0.5	—	—	dB

Note1.Please referto Figure1

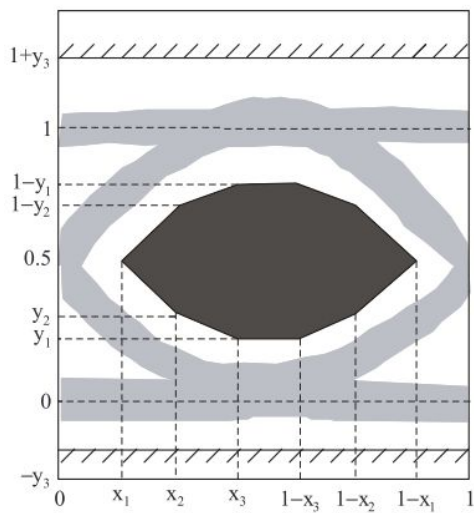


Figure1.Transmissioneyemaskdefinition

Table4 100Gb/s CFP2 Optical Specifications (OTU4)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter</b>						
Channel data rate				27.9525		Gbps
Aggregated data rate				111.809		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	$\lambda_{c0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{c1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{c2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{c3}$		1308.09	1309.14	1310.19	nm
Total Average Launch Power	$P_{out}$		—	—	8.9	dBm
Average Launch Power per Lane	$P_{each}$		-2.5	—	2.9	dBm
Average Launch Power of TX_DIST Transmitter per lane	$P_{off}$	TX_DIS=H	—	—	-30	dBm
Extinction Ratio	$E_R$		7	—	—	dB
SMSR	SMSR		30			dB
Relative Intensity Noise	RIN	Mod off	—	—	-130	dB/Hz
Optical Return Loss Tolerance	$T_{RL}$		—	—	20	dB
Transmitter reflectance	$T_{ef}$		—	—	-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3} <sup>1</sup>	EM		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
<b>Receiver</b>						
Channel data rate				27.9525		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	$\lambda_{R0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{R1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{R2}$		1303.54	1304.58	1305.63	nm

	$\lambda_{R3}$		1308.09	1309.14	1310.19	nm
Damagethreshold	$P_{DT}$		—	5.5	—	dBm
Averagereceiverpowerper lane	Rpow		—	—	4.5	dBm
Optical path penalty					1.5	dB
Receiver Sensitivityperlane <sup>2</sup>	Psen		—	—	-10.3	dBm
ReceiverSensitivity(OMA)perlane <sup>2</sup>	Psen_OMA				-9.1	dBm
Receiver Reflectance	Ref		—	—	-26	dB
Rx-LaneLOSAssert			—	-18	—	dBm
Rx-LaneLOSDeassert			—	-15	—	dBm
Rx-LaneLOSHysteresis			0.5	—	—	dB

Note1.Please referto Figure1

Note2.OTU-4Rate without FEC,BER <math>10^{-12}</math>,ER >7dB

## 2.2 Electricalspecifications

### 2.2.1 HighSpeedI/Ointerface

Table5100Gb/s CFP2ElectricalHighSpeedI/O Interface Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter(CEI-28G-VSRinputinterface)</b>						
SignalRate Per Lane		100GE		25.7812		Gb/s
SignalRate Per Lane		OTU4		27.9525		Gb/s
Differential Input Resistance	Rdin		85	100	115	
Input Impedance Mismatch	Rm				5	%
SinusoidalJitter, Maximum					5	Upp
Sinusoidal Jitter, High Frequency					0.05	Upp
<b>Receiver(CEI-28G-VSRoutputinterface)</b>						
SignalRate Per Lane		100GE		25.7812		Gb/s
SignalRate Per Lane		OTU4		27.9525		Gb/s
Differential Resistance	Rdo		85	100	115	
Uncorrelated Unbounded GaussianJitter				0.1	0.15	Upp
Uncorrelated Bounded High ProbabilityJitter				0.18	0.28	Upp
TotalJitter	T <sub>j</sub>			0.28	0.43	Upp

Note1. Meets CEI-28G-VSRcompliance requirements

## 2.2.2 LowSpeedI/Ointerface

Table6 100Gb/sCFP23.3VLVCMOSElectricalCharacteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SupplyVoltage	Vcc		3.2	3.3	3.4	V
InputHigh Voltage	V <sub>IH</sub>		2		Vcc+0.3	V
InputLowVoltage	V <sub>IL</sub>		-0.3		0.8	V
InputLeakage Current	I <sub>IN</sub>		-10		+10	mA
OutputHigh Voltage (I <sub>OH</sub> =-100uA)	V <sub>OH</sub>		Vcc-0.2		Vcc+0.3	V
OutputLowVoltage (I <sub>OL</sub> =100uA)	V <sub>OL</sub>		-0.3		0.2	V
Minimum Pulse Width of Control Pin Signal	t <sub>CNTL</sub>		100			us

Note.(MOD\_RSTn,MOD\_LOPWR,TX\_DIS,PRG\_CNTL,MOD\_ABS,RX\_LOS, GLB\_ALRMn, PRG\_ALRM )are LVCMOSI/O interfaces.

Table7 100Gb/sCFP21.2VLVCMOSElectricalCharacteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
InputHigh Voltage	V <sub>IH</sub>		0.84		1.5	V
InputLowVoltage	V <sub>IL</sub>		-0.3		0.36	V
InputLeakage Current	I <sub>IN</sub>		-100		+100	uA
OutputHigh Voltage	V <sub>OH</sub>		1.0		1.5	V
OutputLowVoltage	V <sub>OL</sub>		-0.3		0.2	V
OutputHigh Current	I <sub>OH</sub>				-4	mA
Output LowCurrent	I <sub>OL</sub>		+4			mA
Inputcapacitance	C <sub>i</sub>				10	pF

Note.(MDIO,MDC,PRTADR2:0)are 1.2VLVCMOSI/Ointerfaces

Table8 100Gb/s CFP2TimingParametersfor CFP2Hardware SignalPins

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Hardware MOD_LOPWR assert	t <sub>MOD_LOPWR_assert</sub>				1	ms
Hardware MOD_LOPWR deassert	t <sub>MOD_LOPWR_deassert</sub>				10	s
ReceiverLossofSignal AssertTime	t <sub>loss_assert</sub>				100	us <sup>1</sup>

ReceiverLossOfSignal De-AssertTime	t_loss_deassert				100	us <sup>1</sup>
GlobalAlarmAssertDelay Time	GLB_ALRMn_assert				150	ms
Global Alarm De-Assert DelayTime	GLB_ALRMn_deassert				150	ms
Management InterfaceClock Period	t_prd		250			ns
Host MDIOt_setup	t_setup		10			ns

Host MDIO t_hold	t_hold		10			ns
CFP2 MDIOt_delay	t_delay		0		175	ns
Initialization time fromReset	t_initialize				2.5	s
TransmitterDisabled (TX_DISasserted)	t_deassert				100	us
TransmitterEnabled (TX_DISde-asserted)	t_assert				2	ms

Note1. Maximumvalue designed to support telecom applications

Table 9100Gb/sCFP2MDIO andMDCTimingCharacteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
ManagementInterfaceClock Frequency	F_MDC		0.1		4	MHz
ManagementInterfaceClock Period	t_prd		250		10000	ns
Host MDIOt_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP2 MDIOt_delay <sup>1</sup>	t_delay		0		175	ns
MDChigh and lowtime	twidth		40		60	%
			160			ns
MDIO/MDC termination in CFP2	Zt		100			kOhm

Note1.DelayfromMDCrising edge to MDIO data change



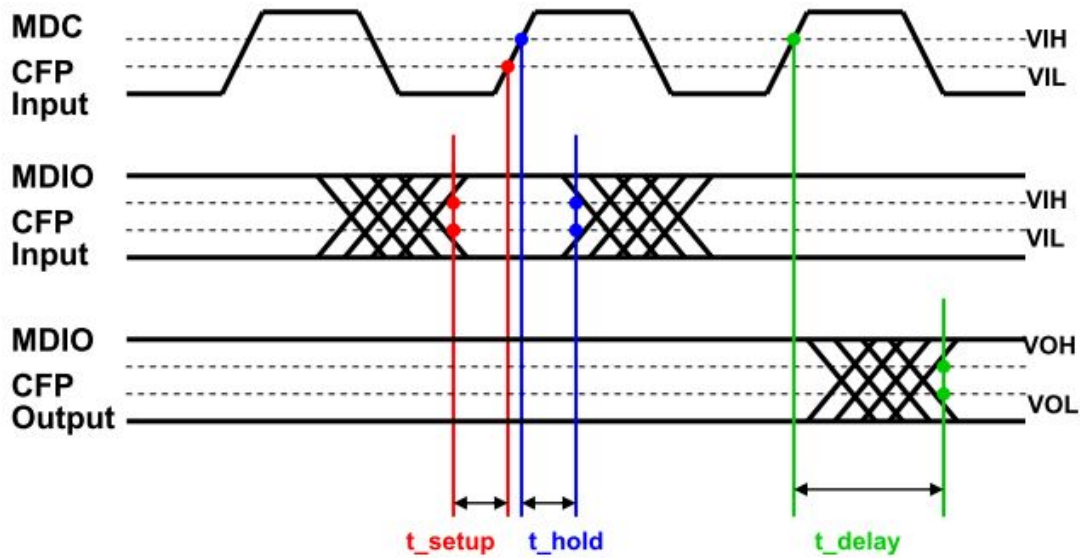


Figure2. 100Gb/sCFP2MDIO &MDCTiming Diagram

### 2.2.3 Clock interface(Optional)

Table 10100Gb/sCFP2ReferenceClockCharacteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Impedance	Zd		80	100	120	ohm
Frequency			1/40 of hostlanerate			
FrequencyStability	Xf		-100		+100	ppm <sup>1</sup>
			-20		+20	ppm <sup>2</sup>
InputDifferential Voltage	Vdiff		400		1200	mV <sup>3</sup>
RMSJitter	$\sigma$				10	ps <sup>4</sup>
ClockDuty Cycle			40		60	%
ClockRise/FallTime10/90%	Tr/f		200		1250	ps <sup>5</sup>

Note1.ForEthernet

applicationsNote2.ForTelecomap

plicationsNote3.Peakto

PeakDifferential

Note4.RandomJitter.Overfrequencyband of10kHz<f <10MHzNote5. 1/40

ofelectricallane

## 3 100Gb/sCFP2FunctionDiagram

### 3.1 Internalreferencestructure

The internal structure of 100Gb/s CFP2 shown as Figure3.

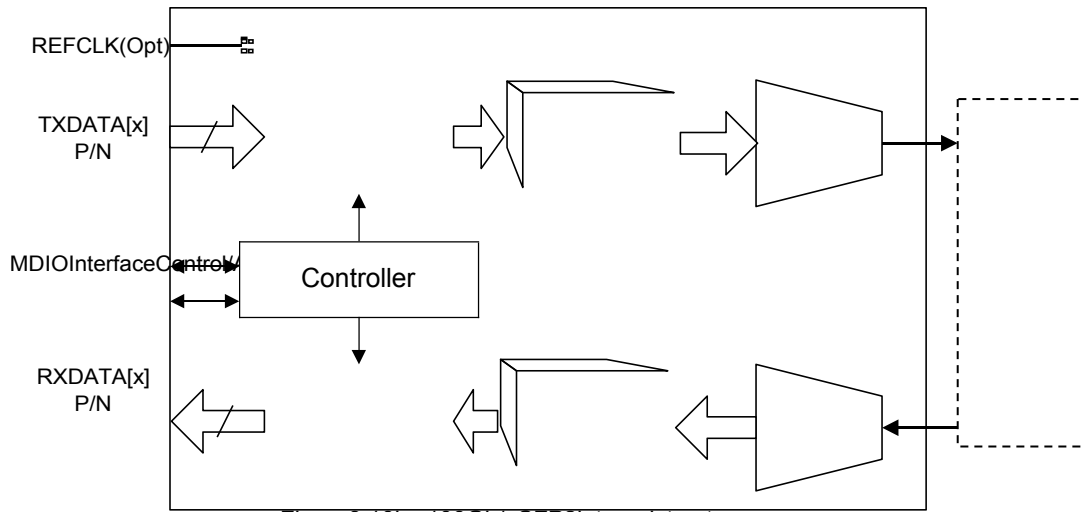


Figure3.10km100Gb/sCFP2internalstructure

### 3.2 Recommended Interface Circuit

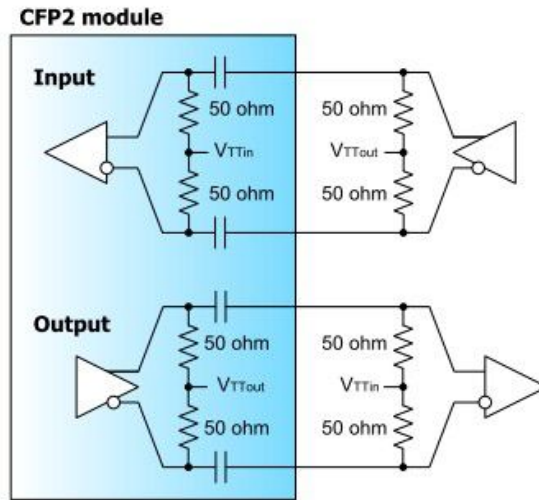


Figure4. Recommended High Speed I/O for Data and Clocks

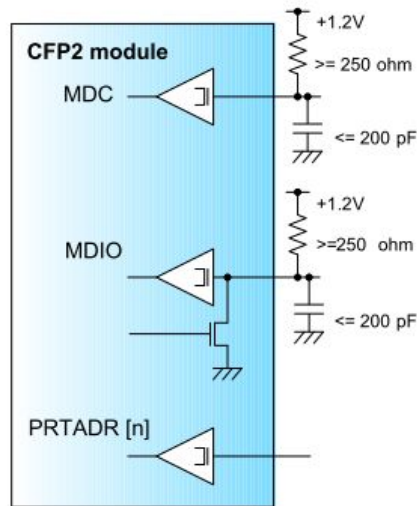


Figure5. Recommended MDIO Interface Termination

### 3.3 Pinlayout

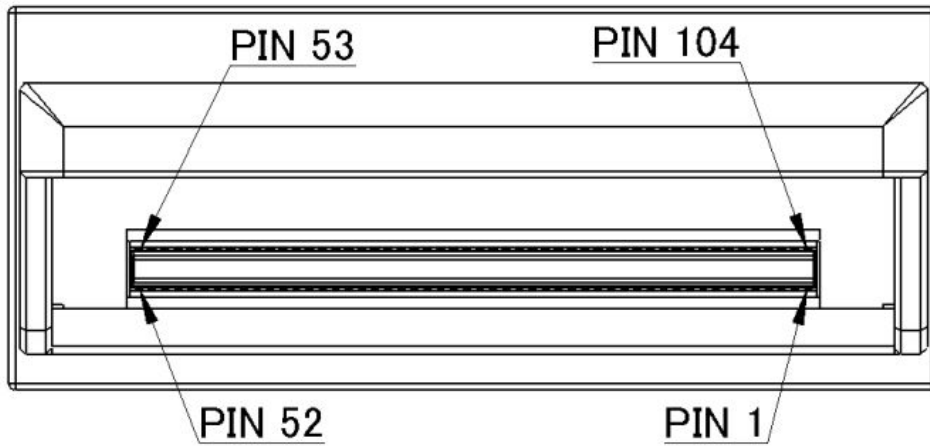


Figure6. CFP2ConnectorPinMap Orientation

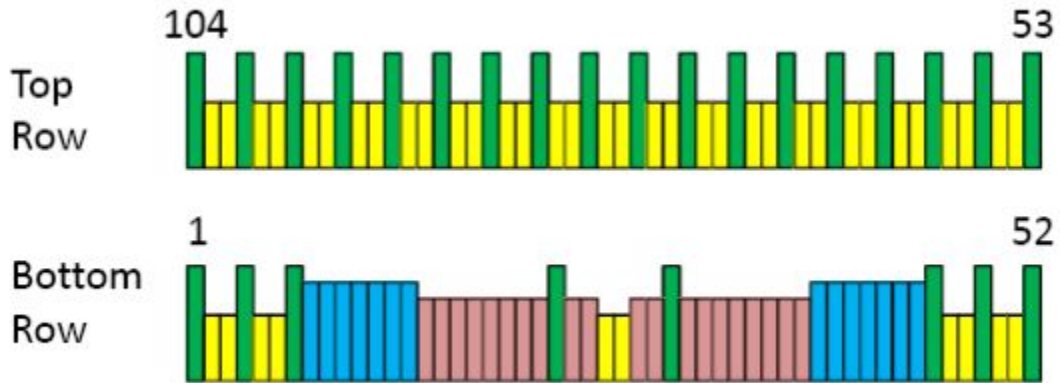


Figure7. CFP2PinMap Connector

Bottom (Nx25G)		Top (4x25G)		Top (8x25G)	
1	GND	104	GND		GND
2	(TX_MCLKn)	103	N.C.		TX7n
3	(TX_MCLKp)	102	N.C.		TX7p
4	GND	101	GND		GND
5	N.C.	100	TX3n		TX6n
6	N.C.	99	TX3p		TX6p
7	3.3V_GND	98	GND		GND
8	3.3V_GND	97	TX2n		TX5n
9	3.3V	96	TX2p		TX5p
10	3.3V	95	GND		GND
11	3.3V	94	N.C.		TX4n
12	3.3V	93	N.C.		TX4p
13	3.3V_GND	92	GND		GND
14	3.3V_GND	91	N.C.		TX3n
15	VND IO A	90	N.C.		TX3p
16	VND IO B	89	GND		GND
17	PRG_CNTL1	88	TX1n		TX2n
18	PRG_CNTL2	87	TX1p		TX2p
19	PRG_CNTL3	86	GND		GND
20	PRG_ALARM1	85	TX0n		TX1n
21	PRG_ALARM2	84	TX0p		TX1p
22	PRG_ALARM3	83	GND		GND
23	GND	82	N.C.		TX0n
24	TX_Dis	81	N.C.		TX0p
25	RX_LOS	80	GND		GND
26	MOD_LOPWR	79	(REFCLKn)		(REFCLKn)
27	MOD_ABS	78	(REFCLKp)		(REFCLKp)
28	MOD_RSTn	77	GND		GND
29	GLB_ALRMn	76	N.C.		RX7n
30	GND	75	N.C.		RX7p
31	MDC	74	GND		GND
32	MDIO	73	RX3n		RX6n
33	PRTADR0	72	RX3p		RX6p
34	PRTADR1	71	GND		GND
35	PRTADR2	70	RX2n		RX5n
36	VND IO C	69	RX2p		RX5p
37	VND IO D	68	GND		GND
38	VND IO E	67	N.C.		RX4n
39	3.3V_GND	66	N.C.		RX4p
40	3.3V_GND	65	GND		GND
41	3.3V	64	N.C.		RX3n
42	3.3V	63	N.C.		RX3p
43	3.3V	62	GND		GND
44	3.3V	61	RX1n		RX2n
45	3.3V_GND	60	RX1p		RX2p
46	3.3V_GND	59	GND		GND
47	N.C.	58	RX0n		RX1n
48	N.C.	57	RX0p		RX1p
49	GND	56	GND		GND
50	(RX_MCLKn)	55	N.C.		RX0n
51	(RX_MCLKp)	54	N.C.		RX0p
52	GND	53	GND		GND

REFCLK (Optional)
----------------------

Figure8. CFP2Module PinMap

Note1: Pin15,16,36,37,38,areinternallyusedandNOTallowedtoconnectany signal

and power supply or GND

Note 2: Pin 2, 3, 50, 51 are disabled unless MCLK output is enabled via MDIO

## 4 100Gb/s CFP2 Mechanical Specifications

100Gb/s CFP2 mechanical dimensions should be compliant with CFP2 MSA specification. Detailed dimensions are shown in Figure 9.

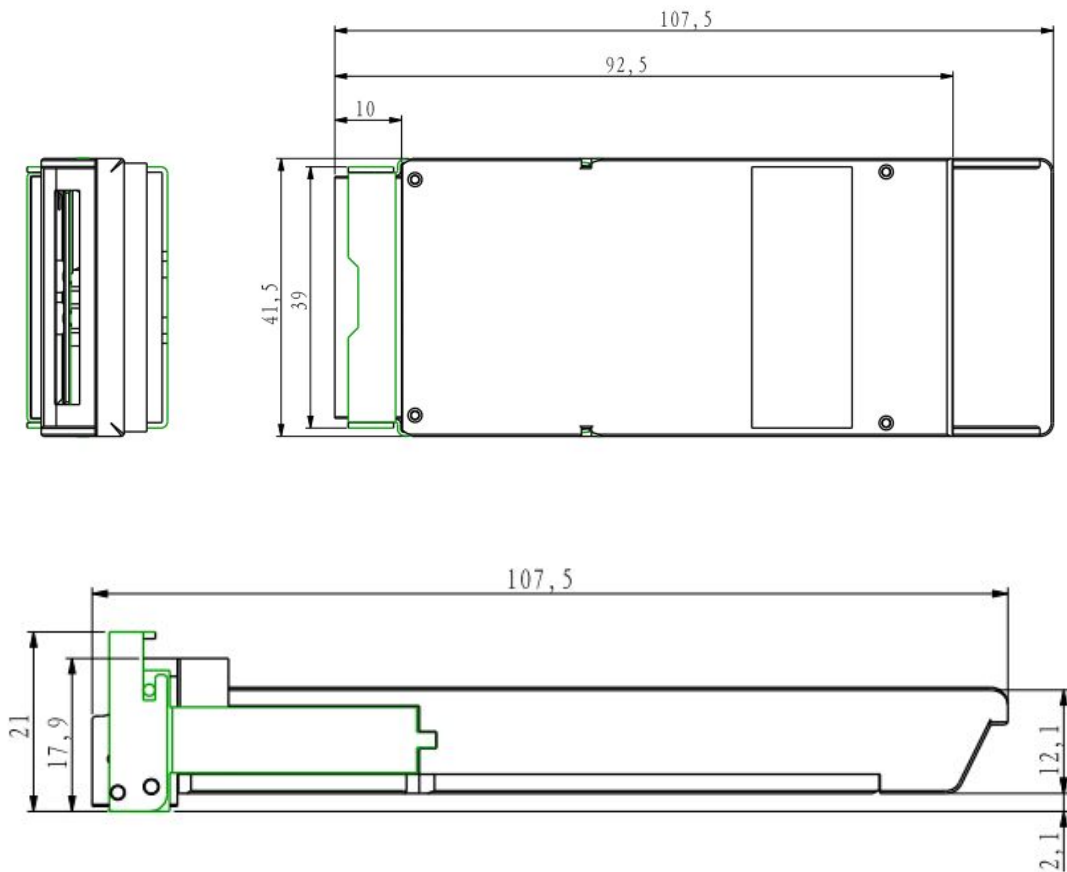
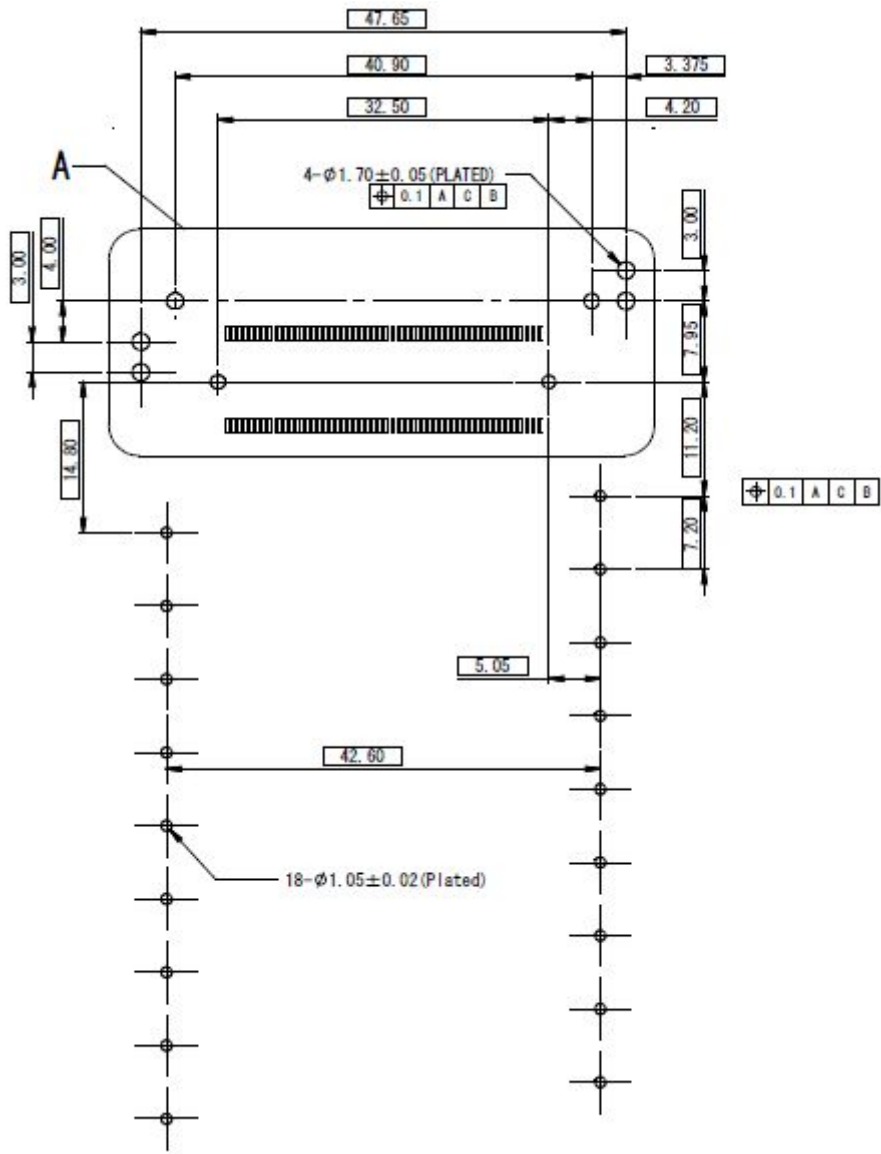


Figure 9. 100Gb/s CFP2 Mechanical Dimensions (unit mm)

The mechanical dimensions of the electrical connectors on the CFP2 Host PCB are shown in Figure 10.



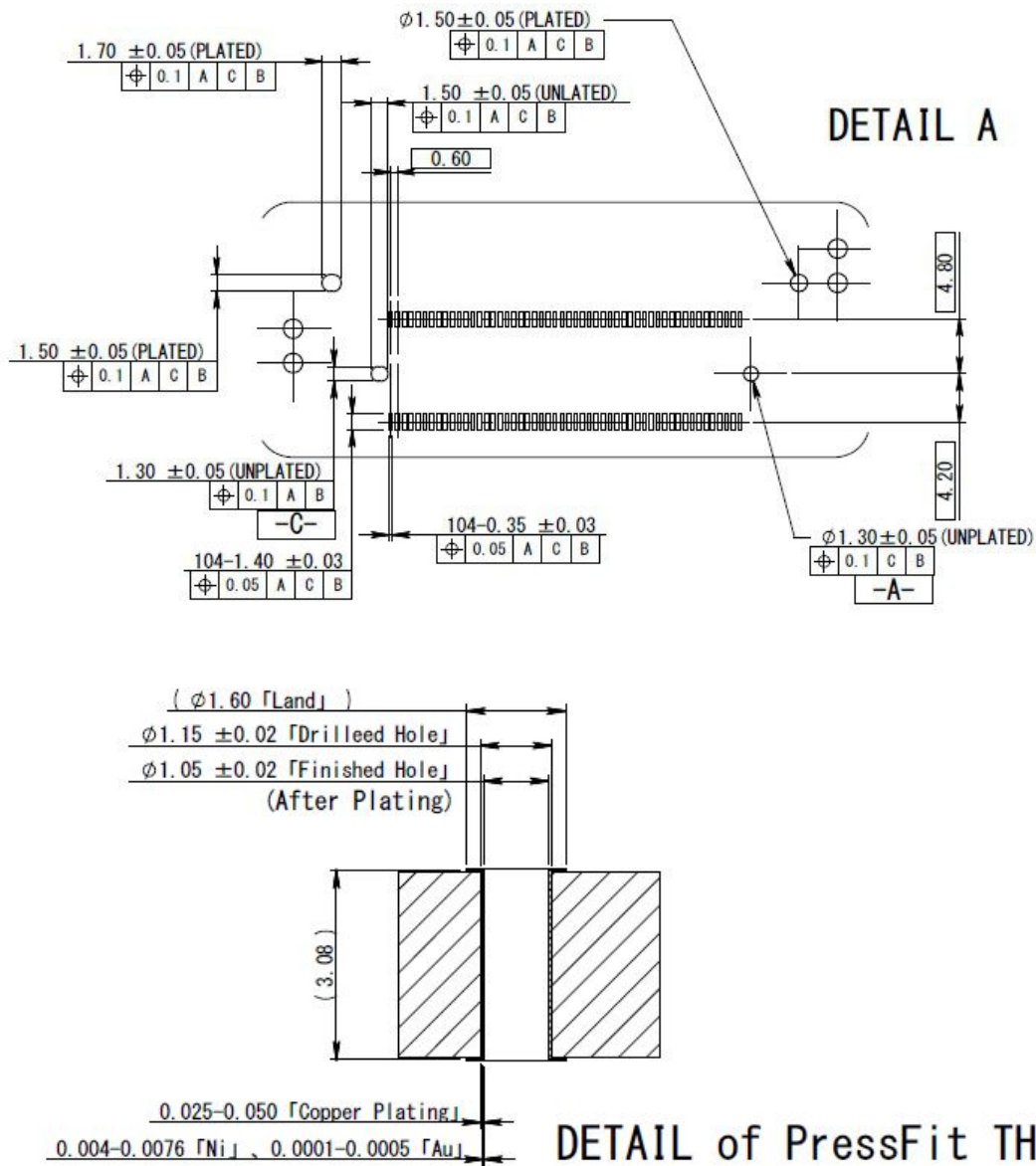


Figure10 MechanicalDimensionsof ElectricalConnectors onCFP2HostPCB(unitmm)

Table11CFP2MechanicalCharacteristics

	Max.	Unit	Notes
Weight	210	g	
Flatness	0.12	mm	
Roughness	1.6	Ra	

Table14 specifyHostConnectorAssemblyInformation for 100Gb/sCFP2 application.

Table 12 HostConnectorAssembly Information (Yamaichi)



PartNumber	Supplier	PartName
CN121S-104-0001	Yamaichi Electronics	Host Connector
CN121A-104-0003	Yamaichi Electronics	AssemblyComponent,incluing Host Connector CoverAssembly
		Cage,Heat Sink, External BracketAssembly

The CFP2 modules support LC optical connector type, The optical connectors are repositioned in the CFP2 module as illustrated in Figure 11.

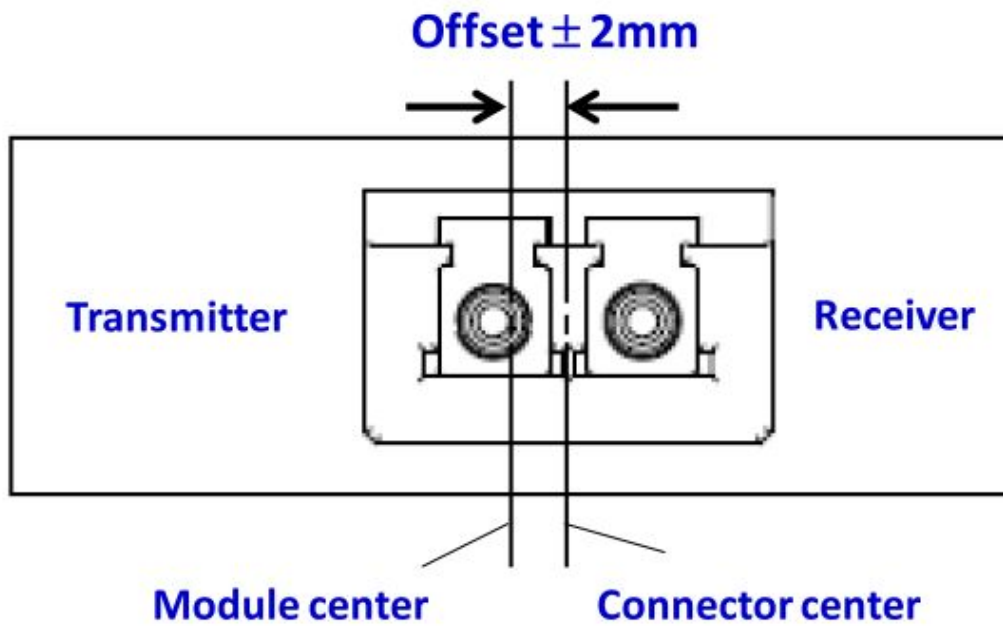


Figure 11 CFP2 Optical Connector Position

## 5 Management Interface

SINOVO SO-100G-CFP2-LR4CFP2 transceivers support the MDIO interface specified in IEEE 802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Three further pins allow for loading of a port address (PORT\_ADDR0-2) into the module.

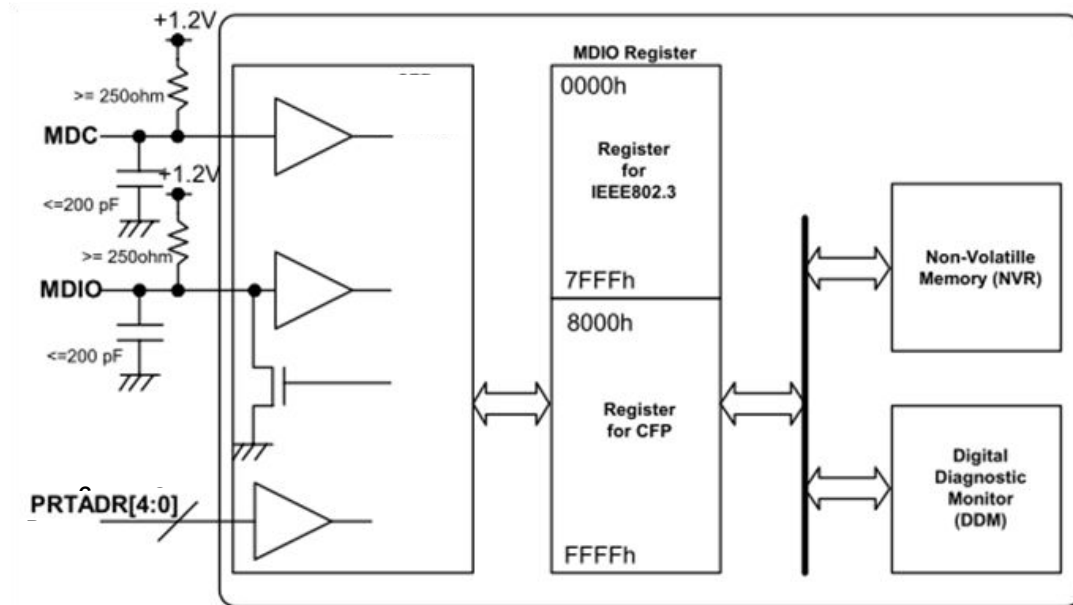


Figure 12 CFP2 MDIO Interface

Note: Capacitor represents stray capacity 600ohm pull-up is preferred  
For more detailed information please refer to "**CFPMSA Management Interface Specification Version 2.2 r06**"

- Notice

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