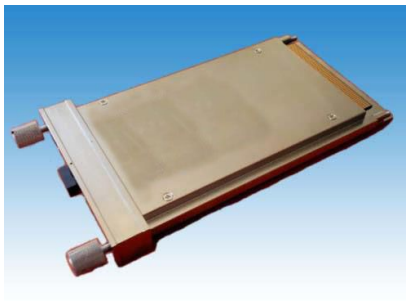
# 100G-BASE-LR410kmCFPOpticalTransceiver

100G-CFP-SR



## Features

- HotPluggableCFPMSApackage
- IEEE 802.3ba 100GBASE-LR4 compliant
- ITU-T4I1-9D1Fcompliant
- CFP-MSA-HW-Spec-rev1-40 compliant
- Up to 10kmforG.652SMF
- Receiver:4-lane x 25Gb/sPINROSAs
- Transmitter: 4-lane x 25Gb/s LAN-WDM EA-DFBTOSAs(1295.56,1300.05,1304.58,1309.14nm)
- 10x10GElectricalSerialInterface (CAUI/OTL4.10)
- MDIOmanagementinterface with DigitalDiagnostic
- +3.3V powersupply
- Powerconsumptionless than 12W
- Compactsize:144.75 x82x 13.6 mm
- Operating case temperature:0to +70 ℃
- Duplex SC orLCReceptacle
- ROHs-6 compliant

## Applications

- 100GBase-LR4 Ethernet
- ITU-TOTU4

## Description

SINOVO 100G-CFP-SR CFPtransceiversaredesignedforusein100GigabitEthernetlinksover10kmsinglemodulefiber, anditcompliantttotheCFPMSAandIEEE802.3ba100GBASE-LR4.DigitaldiagnosticsareavailableviaMDIOasspecifiedintheCFPMSAManagement InterfaceSpecification.

Thetransceiver'sdesignsareoptimizedforhighperformanceandcostefficiencytoprovide customers the bestsolutionsforDatacomandTelecomapplications.

The transceiverisRoHS-6 compliantand lead-free perDirective 2002/95/EC.

## ProductSelection

| 100G-LR4 | |
|---|---|
| SO: | Sinovo |
| TR: | Transceiver |
| 4: | 100Gb/s |
| C1: | CFPSolution 1 |
| L: | 10km |

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# 1 100Gb/s CFPelectrical parameters

## 1.1 AbsoluteMaximumRatings

ThelimitofthemaximumvalueisshownasbelowTable1.(Ifoperatingoutthelimitof themaximumvalue willcause permanent damage).

Table1100Gb/sCFPmodulelimitthemaximum value

| Parameter | Symbol | Conditions | Min. | Max | Unit |
|---|---|---|---|---|---|
| Storagetemperature（case） | $T_{stg}$ | — | -40 | +85 | ℃ |
| Relativehumidity | RH | 0 | — | 85 | % |
| DamageThresholdfor Receiver | Pmax | — | — | +10.0 | dBm |
| Power Supply | Vcc3.3V | — | -0.3 | +3.6 | V |
| | Vcc5.0V | — | — | — | V |
| Input3.3V LVCMOS signal level | Vi | — | -0.3 | Vcc+0.3 | V |
| Input1.2V LVCMOS signal level | Vi | | -0.3 | 1.6 | V |
| ESD Sensitivity onmoduleandallhostpins | HBM | HumanBodymodelR=1.5K, C=100pF | — | 2000 | V |

## 1.2 Recommendedoperatingconditions

Therecommended working conditions are shown asbelowTable2.

Table2100Gb/sCFPrecommendedworkingconditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| OperatingCaseTemperature | Tc | 0 | — | +70 | ℃ |
| Supply voltage | Vcc3.3V | +3.14 | +3.3 | +3.47 | V |
| Supply Current | Icc3.3V | — | — | 3.3 | A |
| Powerdissipation | P | — | — | 12 | W |
| LowPowerdissipation | $P_{Low}$ | | | 2 | W |
| In-rushCurent | I-inrush | | | 50 | mA/us |
| Turn-offrushCurent | I-turnoff | -50 | | | mA/us |
| Link Distance | L | 2M | — | 10km | G.652SMF |

# 2 100Gb/s CFPSpecifications

## 2.1 OpticalSpecifications

Table3100Gb/sCFPOpticalSpecifications(100GBase-LR4)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Transmitter | | | | | | |
| Channeldatarate | | | | 25.7812 | | Gbps |
| Aggregatedatarate | | | | 103.125 | | Gbps |

| | | | | | | |
|---|---|---|---|---|---|---|
| Dataratevariation | | | -100 | | +100 | ppm |
| LaneCenterWavelength | $\lambda c_{T0}$ | | 1294.53 | 1295.56 | 1296.59 | nm |
| | $\lambda c_{T1}$ | | 1299.02 | 1300.05 | 1301.09 | nm |
| | $\lambda c_{T2}$ | | 1303.54 | 1304.58 | 1305.63 | nm |
| | $\lambda c_{T3}$ | | 1308.09 | 1309.14 | 1310.19 | nm |
| TotalAverageLaunchPower | Pout | | — | — | 10.5 | dBm |
| AverageLaunchPowerper Lane | Peach | | -4.3 | — | 4.5 | dBm |
| OpticalModulationAmplitude per Lane | OMA | | -1.3 | — | 4.5 | dBm |
| Differencein Launchpower betweenany twolances(OMA) | | | — | — | 5.0 | dB |
| LaunchpowerinOMAminus TDP, per lane | Pomatdp | | -2.3 | — | — | dBm |
| AverageLaunchPowerof TX_DISTransmitterperlane | Poff | TX_DIS=H | — | — | -30 | dBm |
| ExtinctionRatio | $E_R$ | | 4 | 5.5 | — | dB |
| SMSR | SMSR | | 30 | — | — | dB |
| DispersionPenalty | DP | 10kmSMF | — | — | 2.2 | dB |
| RelativeIntensity Noise | RIN | Modoff | — | — | -130 | dB/Hz |
| OpitcalReturnLossTolerance | $T_{RL}$ | | — | — | 20 | dB |
| Transmitterreflectance | Tef | | — | — | -12 | dB |
| OpticalEyeMask{X1,X2,X3,Y1, Y2,Y3}[1] | EM | | {0.25,0.4,0.45,0.25,0.28, 0.4} | | | |
| **Receiver** | | | | | | |
| Channeldatarate | | | | 25.7812 | | Gbps |
| Dataratevariation | | | -100 | | +100 | ppm |
| LaneCenterWavelength | $\lambda c_{T0}$ | | 1294.53 | 1295.56 | 1296.59 | nm |
| | $\lambda c_{T1}$ | | 1299.02 | 1300.05 | 1301.09 | nm |
| | $\lambda c_{T2}$ | | 1303.54 | 1304.58 | 1305.63 | nm |
| | $\lambda c_{T3}$ | | 1308.09 | 1309.14 | 1310.19 | nm |
| Damagethreshold | $P_{DT}$ | | — | 5.5 | — | dBm |
| Averagereceiverpowerper lane | Rpow | | -10.6 | — | 4.5 | dBm |
| ReceivepowerOMAper Lane | Rovl | | — | — | 4.5 | dBm |
| Differencein receivepower betweenany twolanes(OMA) | | | — | — | 5.5 | dB |
| ReceiverSensitivity(OMA)per lane | Psen | | — | — | -8.6 | dBm |
| StressedReceiverSensitivity per Lane | Psen_str | | — | — | -6.8 | dBm |

| | | | | | | |
|---|---|---|---|---|---|---|
| ReceiverReflectance | Ref | | — | — | -26 | dB |
| Conditionsofstressedreceiversensitivity test | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Verticaleyeclosurepenalty per Lane | | | — | — | 1.8 | dB |
| Stressedeyejitter perLane | | | — | — | 0.3 | UI |
| Rx-LaneLOSAssert | | | — | -18 | — | dBm |
| Rx-LaneLOSDeassert | | | — | -15 | — | dBm |
| Rx-LaneLOSHysteresis | | | 0.5 | — | — | dB |

Note1.Please referto Figure 1

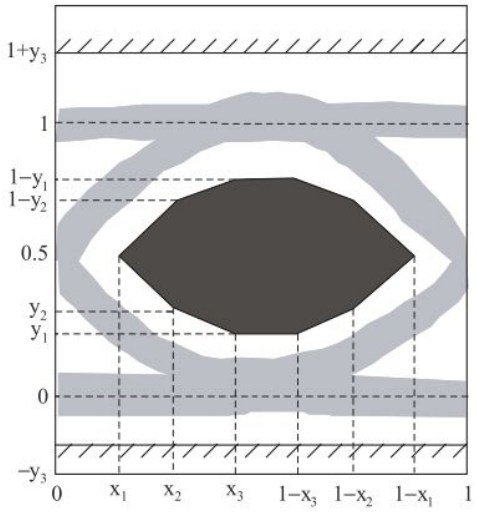


Figure1.Transmissioneyemask definition

Table4100Gb/sCFPOpticalSpecifications(OTU4)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Channeldatarate | | | | 27.9525 | | Gbps |
| Aggregatedatarate | | | | 111.809 | | Gbps |
| Dataratevariation | | | -20 | | +20 | ppm |
| LaneCenterWavelength | $\lambda c_{T0}$ | | 1294.53 | 1295.56 | 1296.59 | nm |
| | $\lambda c_{T1}$ | | 1299.02 | 1300.05 | 1301.09 | nm |
| | $\lambda c_{T2}$ | | 1303.54 | 1304.58 | 1305.63 | nm |
| | $\lambda c_{T3}$ | | 1308.09 | 1309.14 | 1310.19 | nm |
| TotalAverageLaunchPower | Pout | | — | — | 8.9 | dBm |
| AverageLaunchPowerper Lane | Peach | | -2.5 | — | 2.9 | dBm |
| OpticalModulationAmplitude per Lane | OMA | | -1.2 | — | 4.5 | dBm |
| Differencein Launchpower betweenanytwolances(OMA) | | | — | — | 5.0 | dB |
| AverageLaunchPowerof TX_DISTransmitterperlane | Poff | TX_DIS=H | — | — | -30 | dBm |
| ExtinctionRatio | $E_R$ | | 7 | — | — | dB |

| | | | | | | |
|---|---|---|---|---|---|---|
| SMSR | SMSR | | 30 | | | dB |
| RelativeIntensity Noise | RIN | Modoff | — | — | -130 | dB/Hz |
| OpitcalReturnLossTolerance | $T_{RL}$ | | — | — | 20 | dB |
| Transmitterreflectance | Tef | | — | — | -12 | dB |
| OpticalEyeMask{X1,X2,X3,Y1, Y2,Y3}[1] | EM | | {0.25,0.4,0.45,0.25,0.28, 0.4} | | | |
| **Receiver** | | | | | | |
| Channeldatarate | | | | 27.9525 | | Gbps |
| Datarateviation | | | -20 | | +20 | ppm |
| LaneCenterWavelength | $\lambda c_{R0}$ | | 1294.53 | 1295.56 | 1296.59 | nm |
| | $\lambda c_{R1}$ | | 1299.02 | 1300.05 | 1301.09 | nm |
| | $\lambda c_{R2}$ | | 1303.54 | 1304.58 | 1305.63 | nm |
| | $\lambda c_{R3}$ | | 1308.09 | 1309.14 | 1310.19 | nm |
| Damagethreshold | $P_{DT}$ | | — | 5.5 | — | dBm |
| Averagereceiverpowerper lane | Rpow | | — | — | 4.5 | dBm |
| ReceiverpowerOMAper lane | Rovl | | — | — | 4.5 | dBm |
| Differencein receivepower betweenany twolanes(OMA) | | | — | — | 5.5 | dB |
| Opticalpathpenalty | | | | | 1.5 | dB |
| ReceiverSensitivityperlane[2] | Psen | | — | — | -10.3 | dBm |
| ReceiverSensitivity(OMA)perlane[2] | Psen_OMA | | | | -9.1 | dBm |
| ReceiverReflectance | Ref | | — | — | -26 | dB |
| Rx-LaneLOSAssert | | | — | -18 | — | dBm |
| Rx-LaneLOSDeassert | | | — | -15 | — | dBm |
| Rx-LaneLOSHysteresis | | | 0.5 | — | — | dB |

Note1.Please referto Figure 1

Note2.OTU-4Rate, BER<$10^{-12}$with FEC,ER >7dB

## 2.2 Electricalspecifications

### 2.2.1 High Speed I/O interface

Table5100Gb/sCFPElectricalHighSpeedI/O InterfaceSpecifications

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Transmitter(CAUI input interface)** | | | | | | |
| SignalRatePerLane | | | | 10.3125 | | Gb/s |
| SignalRateTolerance | | | -100 | | 100 | ppm |
| AC CommonModeinput Voltage Tolerance(RMS) | | | | | 20 | mV |
| Differential input return loss | $RI_{diff}$ | IEEE 802.3ba-2010 | SeeEquation(83B–7) | | | dB |
| TotalInputJitterTolerance | $T_{jin}$ | | | | 0.62 | UI |

| | | | | | | |
|---|---|---|---|---|---|---|
| DeterministicInput Jitter Tolerance | $T_{din}$ | | | | 0.42 | UI |
| Transmitter Input Eye Mask(X1,X2) | | | (0.31,0.5) | | | UI[1] |
| Transmitter Input Eye Mask(Y1,Y2) | | | (42.5,425) | | | mV[1] |
| **Receiver (CAUI output interface)** | | | | | | |
| SignalRatePerLane | | | | 10.3125 | | Gb/s |
| SignalRateTolerance | | | -100 | | 100 | ppm |
| Single-ended output voltage | Vosig | | -0.4 | | 4 | V |
| OutputACcommon-mode voltage(RMS) | $V_{ocomAC}$ | | | | 15 | mV |
| Outputtransitiontime | Tr | 20%~80% | 24 | — | — | ps |
| Differentialoutputreturn loss | | IEEE 802.3ba-2010 | SeeEquation(83B–5) | | | dB |
| TotalJitter | $T_j$ | | | | 0.4 | UI |
| DeterministicJitter | $T_{dj}$ | | | | 0.25 | UI |
| ReceiverOutputEyeMask (X1,X2) | | | (0.2, 0.5) | | | UI[2] |
| ReceiverOutputEyeMask (Y1,Y2) | | | (136, 380) | | | mV[2] |

Note1.referto figure

2Note2.referto figure 3

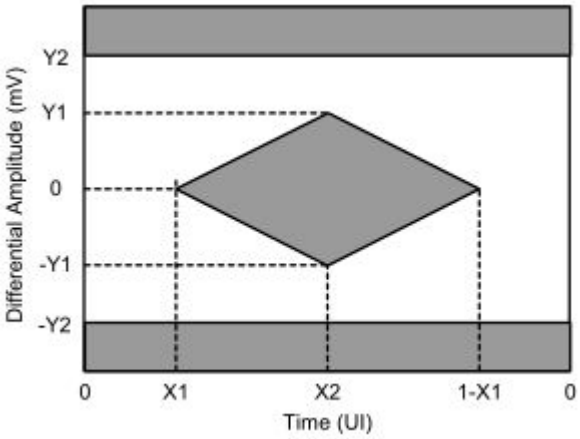


Figure 2.CAUIreceivereyemask

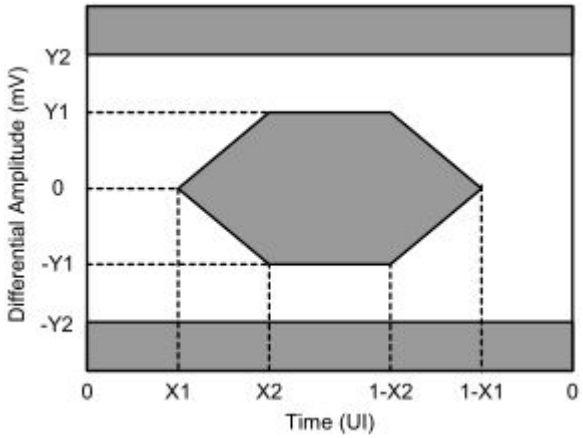


Figure 3.CAUItransmittereye mask

### 2.2.2 LowSpeed I/O interface

Table6100Gb/sCFP3.3V LVCMOSElectricalCharacteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SupplyVoltage | Vcc | | 3.2 | 3.3 | 3.4 | V |
| Input HighVoltage | $V_{IH}$ | | 2 | | Vcc+0.3 | V |
| InputLowVoltage | $V_{IL}$ | | -0.3 | | 0.8 | V |
| InputLeakageCurrent | $I_{IN}$ | | -10 | | +10 | mA |
| OutputHighVoltage ($I_{OH}$=-100uA) | $V_{OH}$ | | Vcc-0.2 | | Vcc+0.3 | V |
| OutputLowVoltage ($I_{OL}$=100uA) | $V_{OL}$ | | -0.3 | | 0.2 | V |
| Minimum Pulse Width of ControlPinSignal | t_CNTL | | 100 | | | us |

Note.(MOD_RSTn,MOD_LOPWR,TX_DIS,PRG_CNTL,MOD_ABS,RX_LOS, GLB_ALRMn, PRG_ALRM ) are LVCMOSI/O interfaces.

Table7100Gb/sCFP1.2V LVCMOSElectricalCharacteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input HighVoltage | $V_{IH}$ | | 0.84 | | 1.5 | V |
| InputLowVoltage | $V_{IL}$ | | -0.3 | | 0.36 | V |
| InputLeakageCurrent | $I_{IN}$ | | -100 | | +100 | uA |
| OutputHighVoltage | $V_{OH}$ | | 1.0 | | 1.5 | V |
| OutputLowVoltage | $V_{OL}$ | | -0.3 | | 0.2 | V |
| OutputHighCurrent | $I_{OH}$ | | | | -4 | mA |
| OutputLowCurrent | $I_{OL}$ | | +4 | | | mA |
| Inputcapacitance | Ci | | | | 10 | pF |

Note.(MDIO,MDC,PRTADR4:0)are 1.2VLVCMOSI/O interfaces

Table8100Gb/sCFPTiming Parameters for CFPHardwareSignalPins

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Hardware | MOD_LOPWR | t_MOD_LOPWR_assert | | | | 1 | ms |

| | | | | | | |
|---|---|---|---|---|---|---|
| assert | | | | | | |
| Hardware MOD_LOPWR deassert | t_MOD_LOPWR_deassert | | | | 10 | s |
| ReceiverLossofSignal AssertTime | t_loss_assert | | | | 100 | us |
| ReceiverLossofSignal De-Assert Time | t_loss_deassert | | | | 100 | us |
| GlobalAlarmAssertDelay Time | GLB_ALRMn_assert | | | | 150 | ms |
| Global Alarm De-Assert DelayTime | GLB_ALRMn_deassert | | | | 150 | ms |
| ManagementInterfaceClock Period | t_prd | | 250 | | | ns |
| Host MDIOt_setup | t_setup | | 10 | | | ns |
| Host MDIOt_hold | t_hold | | 10 | | | ns |
| CFPMDIOt_delay | t_delay | | 0 | | 175 | ns |
| InitializationtimefromReset | t_initialize | | | | 2.5 | s |
| TransmitterDisabled (TX_DIS asserted) | t_deassert | | | | 100 | us |
| TransmitterEnabled (TX_DISde-asserted) | t_assert | | | | 2 | ms |

Table9100Gb/sCFPMDIOandMDCTimingCharacteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ManagementInterfaceClock Frequency | F_MDC | | 0.1 | | 4 | MHz |
| ManagementInterfaceClock Period | t_prd | | 250 | | 10000 | ns |
| Host MDIOt_setup | t_setup | | 10 | | | ns |
| Host MDIOt_hold | t_hold | | 10 | | | ns |
| CFPMDIO t_delay[1] | t_delay | | 0 | | 175 | ns |
| MDC highandlowtime | twidth | | 40<br>160 | | 60 | %<br>ns |
| MDIO/MDCterminationinCFP | Zt | | 100 | | | kOhm |

Note1.DelayfromMDCrising edge to MDIO datachange

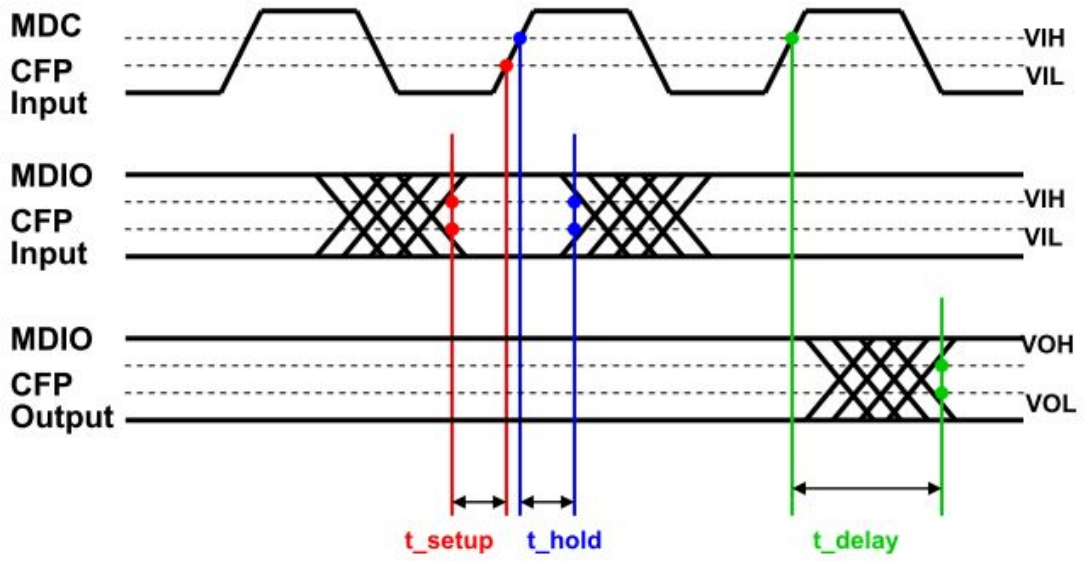


Figure4. 100Gb/sCFPMDIO&MDCTimingDiagram

### 2.2.3 Clock interface

Table10100Gb/sCFPReferenceClockCharacteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Impedance | Zd | | 80 | 100 | 120 | ohm |
| Frequency | | | 1/64ofhostlanerate | | | |
| Frequency Stability | Xf | | -100 | | +100 | ppm[1] |
| | | | -20 | | +20 | ppm[2] |
| Input DifferentialVoltage | Vdiff | | 400 | | 1200 | mV[3] |
| RMS Jitter | σ | | | | 10 | ps[4] |
| Clock Duty Cycle | | | 40 | | 60 | % |
| Clock Rise/FallTime10/90% | Tr/f | | 200 | | 1250 | ps[5] |

Note1.ForEthernetapplicationsN
ote2.ForTelecomapplicationsNot
e3.Peakto PeakDifferential
Note4.RandomJitter.Overfrequencyband of 10kHz<f <10MHzNote5.
1/64of electricallane

Table11100Gb/sCFPTransmitter&ReceiverMonitorClock Characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Impedance | Zd | | 80 | 100 | 120 | ohm |
| Frequency | | | 1/8ofnetworklanerate | | | |
| OuputDifferentialVoltage | Vdiff | | 400 | | 1200 | mV[1] |
| Clock Duty Cycle | | | 40 | | 60 | % |

Note1.Peakto PeakDifferential

# 3 100Gb/s CFPFunctionDiagram

## 3.1 Internalreferencestructure

The internalstructure of100Gb/s CFPshown as Figure 5.

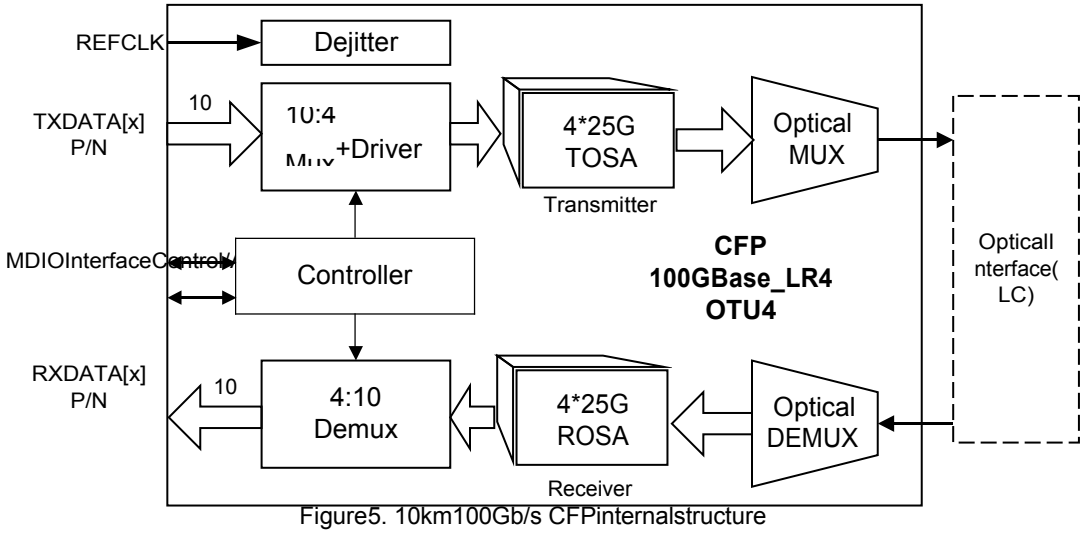


Figure5. 10km100Gb/s CFPinternalstructure

## 3.2 RecommendedInterfaceCircuit

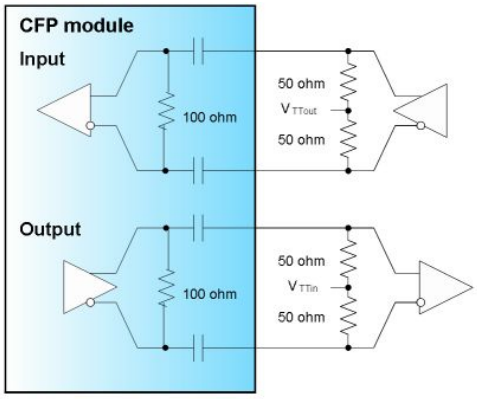


Figure6. RecommendedHighSpeedI/O for DataandClocks

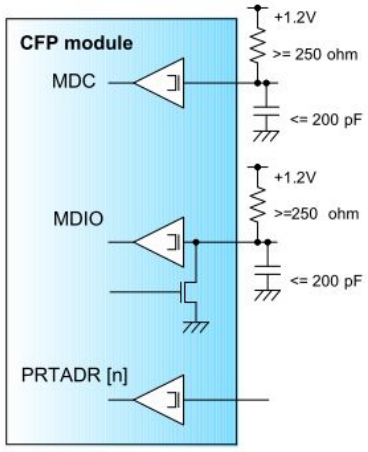

Figure7. RecommendedMDIO InterfaceTermination




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## 3.3 Pin layout

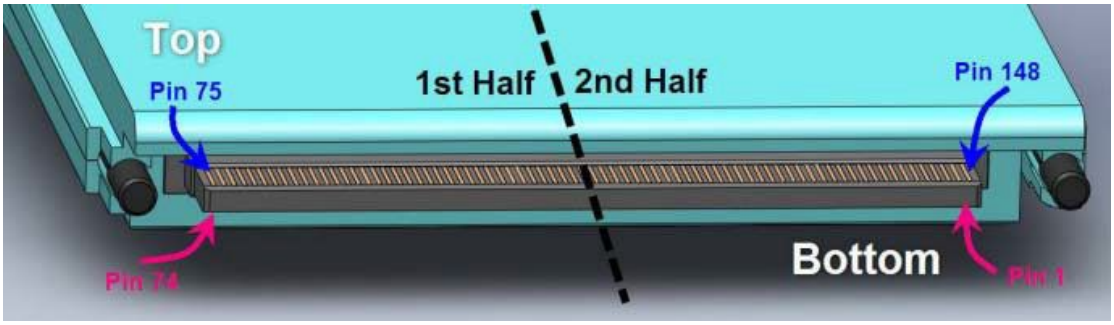


Figure8. CFPModulePadLayout

| | Top Row (2nd Half) | | Bottom Row (2nd Half) |
|---|---|---|---|
| 148 | GND | 1 | 3.3V_GND |
| 147 | REFCLKn | 2 | 3.3V_GND |
| 146 | REFCLKp | 3 | 3.3V_GND |
| 145 | GND | 4 | 3.3V_GND |
| 144 | N.C. | 5 | 3.3V_GND |
| 143 | N.C. | 6 | 3.3V |
| 142 | GND | 7 | 3.3V |
| 141 | TX9n | 8 | 3.3V |
| 140 | TX9p | 9 | 3.3V |
| 139 | GND | 10 | 3.3V |
| 138 | TX8n | 11 | 3.3V |
| 137 | TX8p | 12 | 3.3V |
| 136 | GND | 13 | 3.3V |
| 135 | TX7n | 14 | 3.3V |
| 134 | TX7p | 15 | 3.3V |
| 133 | GND | 16 | 3.3V_GND |
| 132 | TX6n | 17 | 3.3V_GND |
| 131 | TX6p | 18 | 3.3V_GND |
| 130 | GND | 19 | 3.3V_GND |
| 129 | TX5n | 20 | 3.3V_GND |
| 128 | TX5p | 21 | VND_IO_A |
| 127 | GND | 22 | VND_IO_B |
| 126 | TX4n | 23 | GND |
| 125 | TX4p | 24 | *(TX_MCLKn)* |
| 124 | GND | 25 | *(TX_MCLKp)* |
| 123 | TX3n | 26 | GND |
| 122 | TX3p | 27 | VND_IO_C |
| 121 | GND | 28 | VND_IO_D |
| 120 | TX2n | 29 | VND_IO_E |
| 119 | TX2p | 30 | PRG_CNTL1 |
| 118 | GND | 31 | PRG_CNTL2 |
| 117 | TX1n | 32 | PRG_CNTL3 |
| 116 | TX1p | 33 | PRG_ALRM1 |
| 115 | GND | 34 | PRG_ALRM2 |
| 114 | TX0n | 35 | PRG_ALRM3 |
| 113 | TX0p | 36 | TX_DIS |
| 112 | GND | 37 | MOD_LOPWR |

| | Top Row (1st Half) | | Bottom Row (1st Half) |
|---|---|---|---|
| 111 | GND | 38 | MOD_ABS |
| 110 | N.C. | 39 | MOD_RSTn |
| 109 | N.C. | 40 | RX_LOS |
| 108 | GND | 41 | GLB_ALRMn |
| 107 | RX9n | 42 | PRTADR4 |
| 106 | RX9p | 43 | PRTADR3 |
| 105 | GND | 44 | PRTADR2 |
| 104 | RX8n | 45 | PRTADR1 |
| 103 | RX8p | 46 | PRTADR0 |
| 102 | GND | 47 | MDIO |
| 101 | RX7n | 48 | MDC |
| 100 | RX7p | 49 | GND |
| 99 | GND | 50 | VND_IO_F |
| 98 | RX6n | 51 | VND_IO_G |
| 97 | RX6p | 52 | GND |
| 96 | GND | 53 | VND_IO_H |
| 95 | RX5n | 54 | VND_IO_J |
| 94 | RX5p | 55 | 3.3V_GND |
| 93 | GND | 56 | 3.3V_GND |
| 92 | RX4n | 57 | 3.3V_GND |
| 91 | RX4p | 58 | 3.3V_GND |
| 90 | GND | 59 | 3.3V_GND |
| 89 | RX3n | 60 | 3.3V |
| 88 | RX3p | 61 | 3.3V |
| 87 | GND | 62 | 3.3V |
| 86 | RX2n | 63 | 3.3V |
| 85 | RX2p | 64 | 3.3V |
| 84 | GND | 65 | 3.3V |
| 83 | RX1n | 66 | 3.3V |
| 82 | RX1p | 67 | 3.3V |
| 81 | GND | 68 | 3.3V |
| 80 | RX0n | 69 | 3.3V |
| 79 | RX0p | 70 | 3.3V_GND |
| 78 | GND | 71 | 3.3V_GND |
| 77 | *(RX_MCLKn)* | 72 | 3.3V_GND |
| 76 | *(RX_MCLKp)* | 73 | 3.3V_GND |
| 75 | GND | 74 | 3.3V_GND |

Figure9. CFPModulePinMap

Note1:Pin21,22,27,28,29,50,51,53,54areinternallyusedand NOTallowedtoconnectanysignaland powersupplyor GND

Note2:Pin24,25,76,77are disabled unless MCLK outputis enabled via MDIO

## 3.4 Pin definition

Table12100Gb/sCFPPinDefinition(Bottomraw)




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| PIN | Name | I/O | Logic | Description |
|---|---|---|---|---|
| 1 | 3.3V_GND | | | 3.3V ModuleSupply VoltageReturnGround,canbeseparateor tiedtogetherwithSignalGround |
| 2 | 3.3V_GND | | | |
| 3 | 3.3V_GND | | | |
| 4 | 3.3V_GND | | | |
| 5 | 3.3V_GND | | | |
| 6 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 7 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 8 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 9 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 10 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 11 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 12 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 13 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 14 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 15 | 3.3V | | | 3.3V ModuleSupplyVoltage |
| 16 | 3.3V_GND | | | 3.3V ModuleSupply VoltageReturnGround,canbeseparateor tiedtogetherwithSignalGround |
| 17 | 3.3V_GND | | | |
| 18 | 3.3V_GND | | | |
| 19 | 3.3V_GND | | | |
| 20 | 3.3V_GND | | | |
| 21 | VND_IO_A | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 22 | VND_IO_B | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 23 | GND | | | |
| 24 | TX_MCLKn | O | CML | TX MonitorClockOutput(Negative) |
| 25 | TX_MCLKp | O | CML | TX MonitorClockOutput(Positive) |
| 26 | GND | | | |
| 27 | VND_IO_C | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 28 | VND_IO_D | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 29 | VND_IO_E | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 30 | PRG_CNTL1 | I | LVCMOS w/PUR | ProgrammableControl1set overMDIO,MSADefault:TRXIC_RSTn, TX& RXICsreset,"0":reset,"1"orNC:enabled=not used 4.75kohmpullupinthemodule |
| 31 | PRG_CNTL2 | I | LVCMOS w/PUR | ProgrammableControl2set overMDIO,MSADefault:HardwareInterlock LSB,"00":≤8W,"01":≤16W,"10":≤24W,"11"orNC:≤32W =not used |

| | | | | |
|---|---|---|---|---|
| 32 | PRG_CNTL3 | I | LVCMOS w/PUR | ProgrammableControl3set overMDIO,MSADefault:HardwareInterlockMSB,"00":≤8W,"01":≤16W,"10":≤24W,"11"or NC:≤32W=notused |
| 33 | PRG_ALRM1 | | LVCMOS | ProgrammableAlarm 1set overMDIO,MSADefault: |

| | | | | |
|---|---|---|---|---|
| | | O | | HIPWR_ON,"1":modulepower upcompleted,"0": modulenothighpoweredup |
| 34 | PRG_ALRM2 | O | LVCMOS | ProgrammableAlarm 2set overMDIO,MSADefault: MOD_READY,"1": Ready,"0": not Ready. |
| 35 | PRG_ALRM3 | O | LVCMOS | ProgrammableAlarm 3set overMDIO,MSADefault: MOD_FAULT, fault detected,"1":Fault,"0":NoFault |
| 36 | TX_DIS | I | LVCMOS w/PUR | TransmitterDisableforalllanes,"1"or NC= transmitterdisabled,"0"=transmitterenabled |
| 37 | MOD_LOPWR | I | LVCMOS w/PUR | ModuleLowPowerMode."1"or NC:moduleinlow power (safe)mode,"0":power-onenabled4.75kohmpullupinthemodule |
| 38 | MOD_ABS | O | GND | ModuleAbsent."1"orNC:moduleabsent,"0": modulepresent,PullUpResistor onHost |
| 39 | MOD_RSTn | I | LVCMOS w/PDR | ModuleReset."0"resets themodule,"1"or NC =moduleenabled,4.75kohmPullDownResistorin Module |
| 40 | RX_LOS | O | LVCMOS | ReceiverLossofOpticalSignal,"1":lowoptical signal,"0":normalcondition |
| 41 | GLB_ALRMn | O | LVCMOS | GlobalAlarm.“0":alarm conditioninanyMDIOAlarm register,"1":noalarmcondition,OpenDrain,PullUpResistoronHost |
| 42 | PRTADR4 | I | 1.2V CMOS | MDIO PhysicalPortaddressbit 4 |
| 43 | PRTADR3 | I | 1.2V CMOS | MDIO PhysicalPortaddressbit 3 |
| 44 | PRTADR2 | I | 1.2V CMOS | MDIO PhysicalPortaddressbit 2 |
| 45 | PRTADR1 | I | 1.2V CMOS | MDIO PhysicalPortaddressbit 1 |
| 46 | PRTADR0 | I | 1.2V CMOS | MDIO PhysicalPortaddressbit 0 |
| 47 | MDIO | I/O | 1.2V CMOS | ManagementDataI/Obi-directionaldata(electrical specsasper802.3aeandba) |
| 48 | MDC | I | 1.2V CMOS | ManagementDataClock(electricalspecsasper 802.3aeandba) |
| 49 | GND | | | |
| 50 | VND_IO_F | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 51 | VND_IO_G | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 52 | GND | | | |
| 53 | VND_IO_H | I/O | | ModuleVendorI/O.MustNoConnect athostboard |
| 54 | VND_IO_J | I/O | | ModuleVendorI/O.MustNoConnect athostboard |

| | | | | |
|---|---|---|---|---|
| 55 | 3.3V_GND | | | 3.3V ModuleSupply VoltageReturnGround,canbe |
| 56 | 3.3V_GND | | | separateor tiedtogetherwithSignalGround |

| | | | | |
|---|---|---|---|---|
| 57 | 3.3V_GND | | | |
| 58 | 3.3V_GND | | | |
| 59 | 3.3V_GND | | | |
| 60 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 61 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 62 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 63 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 64 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 65 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 66 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 67 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 68 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 69 | 3.3V | | | 3.3V ModuleSupply Voltage |
| 70 | 3.3V_GND | | | |
| 71 | 3.3V_GND | | | |
| 72 | 3.3V_GND | | | 3.3V ModuleSupply |
| 73 | 3.3V_GND | | | VoltageReturnGround,canbeseparateor |
| 74 | 3.3V_GND | | | tiedtogetherwithSignalGround |

Table13100Gb/sCFPPinDefinition(Topraw)

| PIN | Name | I/O | Logic | Description |
|---|---|---|---|---|
| 75 | GND | | | |
| 76 | RX_MCLKp | O | | RXMonitor Clock Output(Positive) |
| 77 | RX_MCLKn | O | | RXMonitor Clock Output(Negative) |
| 78 | GND | | | |
| 79 | RX0p | O | HS I/O | Lane0ReceiverOutput(Positive) |
| 80 | RX0n | O | HS I/O | Lane0ReceiverOutput(Negative) |
| 81 | GND | | | |
| 82 | RX1p | O | HS I/O | Lane1ReceiverOutput(Positive) |
| 83 | RX1n | O | HS I/O | Lane1ReceiverOutput(Negative) |
| 84 | GND | | | |
| 85 | RX2p | O | HS I/O | Lane2ReceiverOutput(Positive) |
| 86 | RX2n | O | HS I/O | Lane2ReceiverOutput(Negative) |
| 87 | GND | | | |
| 88 | RX3p | O | HS I/O | Lane3ReceiverOutput(Positive) |
| 89 | RX3n | O | HS I/O | Lane3ReceiverOutput(Negative) |
| 90 | GND | | | |
| 91 | RX4p | O | HS I/O | Lane4ReceiverOutput(Positive) |
| 92 | RX4n | O | HS I/O | Lane4ReceiverOutput(Negative) |
| 93 | GND | | | |
| 94 | RX5p | O | HS I/O | Lane5ReceiverOutput(Positive) |

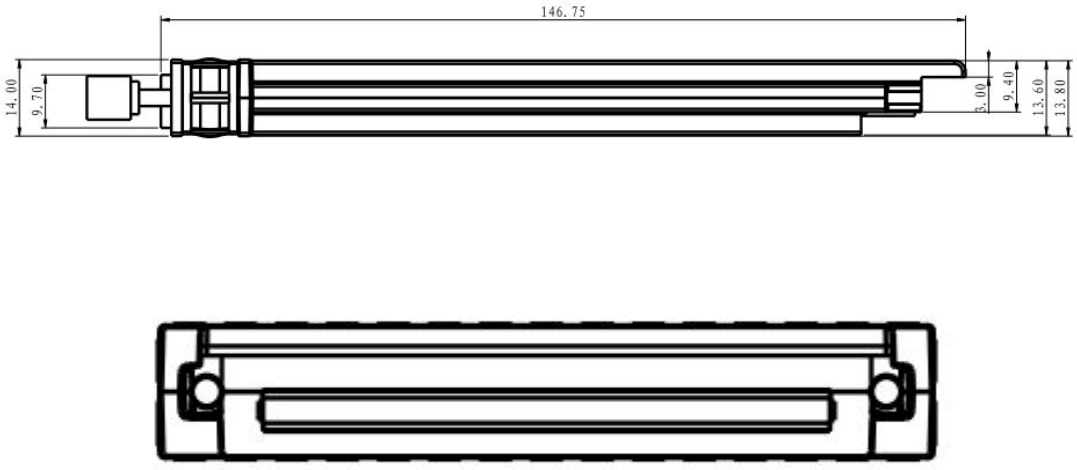
| | | | | |
|---|---|---|---|---|
| 95 | RX5n | O | HS I/O | Lane5ReceiverOutput(Negative) |

| | | | | |
|---|---|---|---|---|
| 96 | GND | | | |
| 97 | RX6p | O | HS I/O | Lane6ReceiverOutput(Positive) |
| 98 | RX6n | O | HS I/O | Lane6ReceiverOutput(Negative) |
| 99 | GND | | | |
| 100 | RX7p | O | HS I/O | Lane7ReceiverOutput(Positive) |
| 101 | RX7n | O | HS I/O | Lane7ReceiverOutput(Negative) |
| 102 | GND | | | |
| 103 | RX8p | O | HS I/O | Lane8ReceiverOutput(Positive) |
| 104 | RX8n | O | HS I/O | Lane8ReceiverOutput(Negative) |
| 105 | GND | | | |
| 106 | RX9p | O | HS I/O | Lane9ReceiverOutput(Positive) |
| 107 | RX9n | O | HS I/O | Lane9ReceiverOutput(Negative) |
| 108 | GND | | | |
| 109 | NC | | | NotConnectedInternally |
| 110 | NC | | | NotConnectedInternally |
| 111 | GND | | | |
| 112 | GND | | | |
| 113 | TX0p | I | HS I/O | Lane0TransmitterInput(Positive) |
| 114 | TX0n | I | HS I/O | Lane0TransmitterInput(Negative) |
| 115 | GND | | | |
| 116 | TX1p | I | HS I/O | Lane1TransmitterInput(Positive) |
| 117 | TX1n | I | HS I/O | Lane1TransmitterInput(Negative) |
| 118 | GND | | | |
| 119 | TX2p | I | HS I/O | Lane2TransmitterInput(Positive) |
| 120 | TX2n | I | HS I/O | Lane2TransmitterInput(Negative) |
| 121 | GND | | | |
| 122 | TX3p | I | HS I/O | Lane3TransmitterInput(Positive) |
| 123 | TX3n | I | HS I/O | Lane3TransmitterInput(Negative) |
| 124 | GND | | | |
| 125 | TX4p | I | HS I/O | Lane4TransmitterInput(Positive) |
| 126 | TX4n | I | HS I/O | Lane4TransmitterInput(Negative) |
| 127 | GND | | | |
| 128 | TX5p | I | HS I/O | Lane5TransmitterInput(Positive) |
| 129 | TX5n | I | HS I/O | Lane5TransmitterInput(Negative) |
| 130 | GND | | | |
| 131 | TX6p | I | HS I/O | Lane6TransmitterInput(Positive) |
| 132 | TX6n | I | HS I/O | Lane6TransmitterInput(Negative) |
| 133 | GND | | | |
| 134 | TX7p | I | HS I/O | Lane7TransmitterInput(Positive) |
| 135 | TX7n | I | HS I/O | Lane7TransmitterInput(Negative) |
| 136 | GND | | | |
| 137 | TX8p | I | HS I/O | Lane8TransmitterInput(Positive) |

| | | | | |
|---|---|---|---|---|
| 138 | TX8n | I | HS I/O | Lane8TransmitterInput(Negative) |
| 139 | GND | | | |
| 140 | TX9p | I | HS I/O | Lane9TransmitterInput(Positive) |
| 141 | TX9n | I | HS I/O | Lane9TransmitterInput(Negative) |
| 142 | GND | | | |
| 143 | NC | | | NotConnectedInternally |
| 144 | NC | | | NotConnectedInternally |
| 145 | GND | | | |
| 146 | REFCLKp | I | | ReferenceClockInput(Positive) |
| 147 | REFCLKn | I | | ReferenceClockInput(Negative) |
| 148 | GND | | | |

# 4 100Gb/s CFP Mechanical Specifications

100Gb/sCFPmechanicaldimensionsshouldbe compliantwithCFPMSAspecification.Detailed dimensions are shownin Figure 10.



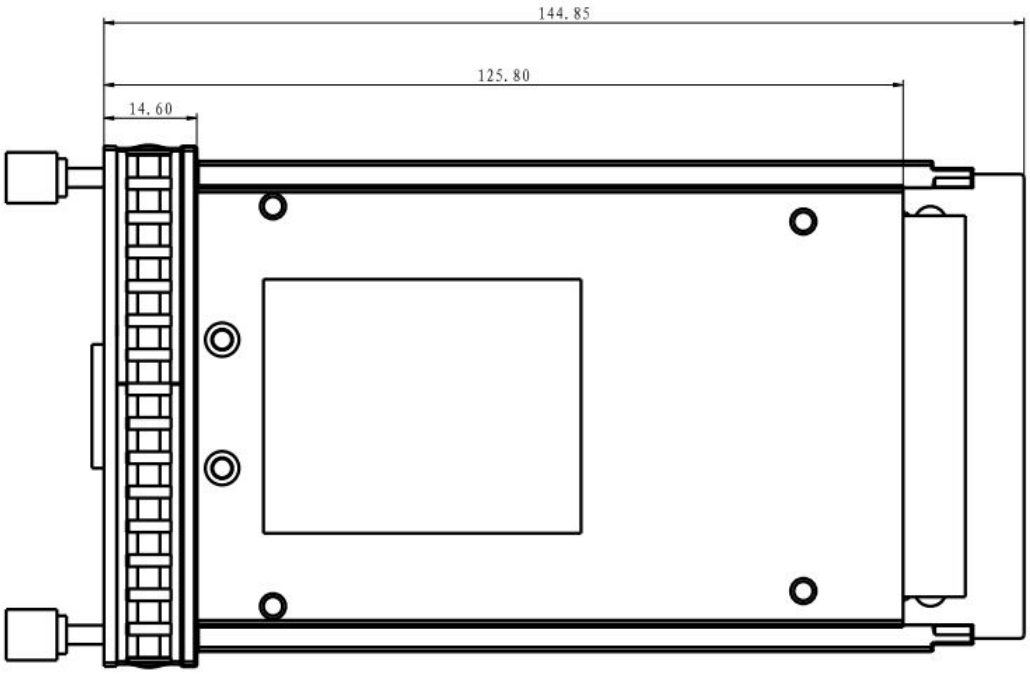



Figure10.100Gb/sCFPMechanicalDimensions(unit:mm)

ThemechanicaldimensionsoftheelectricalconnectorsontheCFPHostPCBareshown in Figure11.

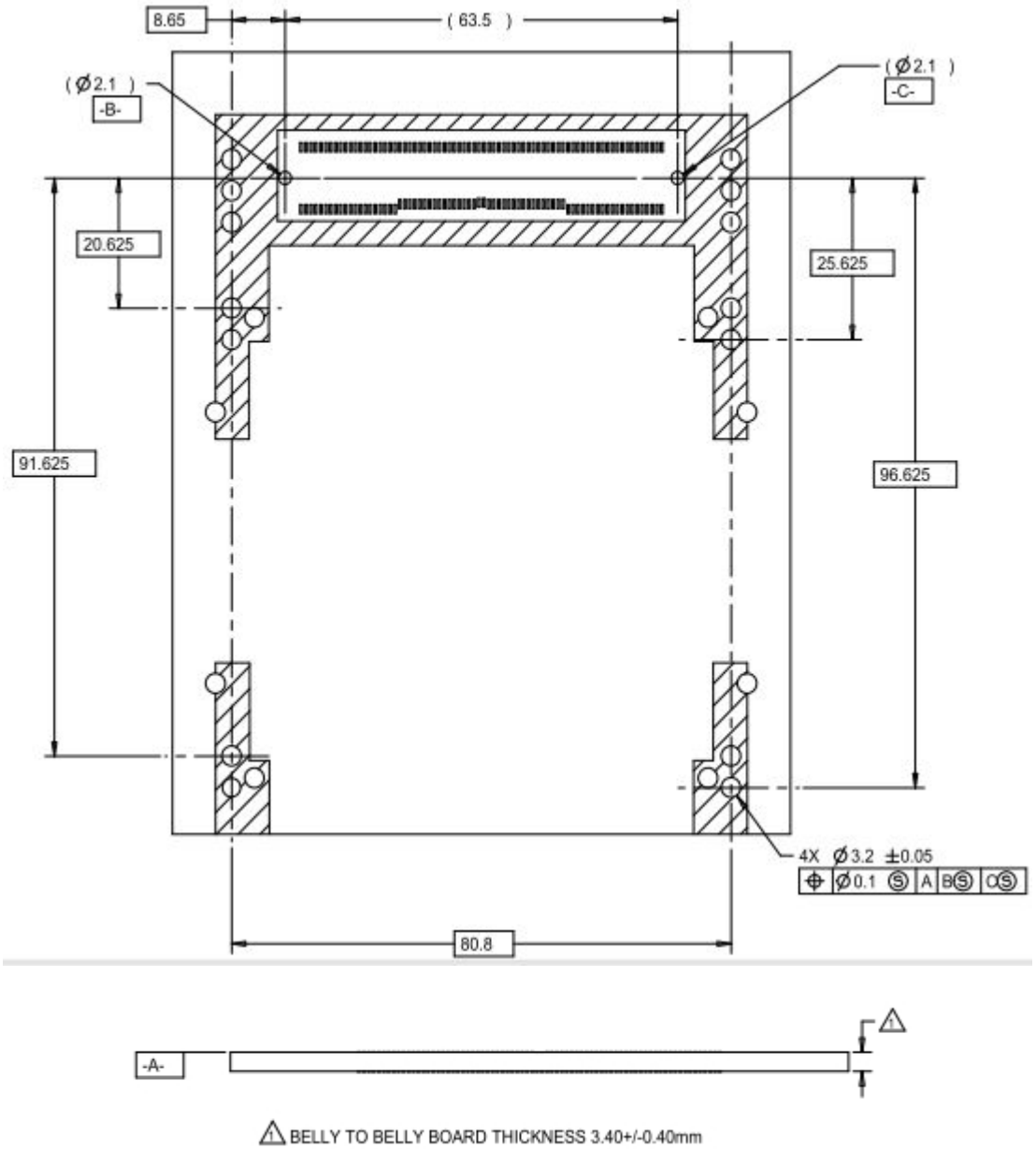



Figure11MechanicalDimensionsofElectricalConnectors onCFPHostPCB

Table14CFPMechanicalCharacteristics

| | Max. | Unit | Notes |
|---|---|---|---|
| Weight | 350 | g | |
| Flatness | 0.15 | mm | |
| Roughness | 6.3 | Ra | |

Table 15/16specifyHostConnectorAssemblyInformationfor100Gb/sCFPapplication.

Table15 HostConnectorAssembly Information（Tyco）

| PartNumber | Supplier | PartName |
|---|---|---|
| 2057626-1 | TycoElectronics | ExternalBracketAssembly |

| | | |
|---|---|---|
| 2057592-2 | TycoElectronics | GuideRail |

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| | | |
|---|---|---|
| 2057631-1 | TycoElectronics | Host ConnectorCoverAssembly |
| 2057930-1 | TycoElectronics | BackerPlateAssembly |
| 2057630-1 | TycoElectronics | Host Connector |

Table16 HostConnectorAssembly Information（Yamaichi）

| PartNumber | Supplier | PartName |
|---|---|---|
| CA009-1203-001 | YamaichiElectronics | ExternalBracketAssembly |
| CA009-1201-001 | YamaichiElectronics | GuideRail |
| CA009-1400-001 | YamaichiElectronics | Host ConnectorCoverAssembly |
| CA009-1204-001 | YamaichiElectronics | BackerPlateAssembly |
| CA009-S001-001 | YamaichiElectronics | Host Connector |

# 5 Management Interface

SINOVO SO-100G-LR4CFPtransceiverssupportstheMDIOinterfacespecifiedinIEEE802.3Clause45.This2-wiremanagementdataI/Ointerfaceisprovidedforthemodulestatusmonitoringandcontrol.The managementdataclock(MDC)providesclockingforthedatathatispassedontheMDIOport.Fivef urtherpinsallowforloadingofa portaddress (PORT_ADDR0-4) into themodule.

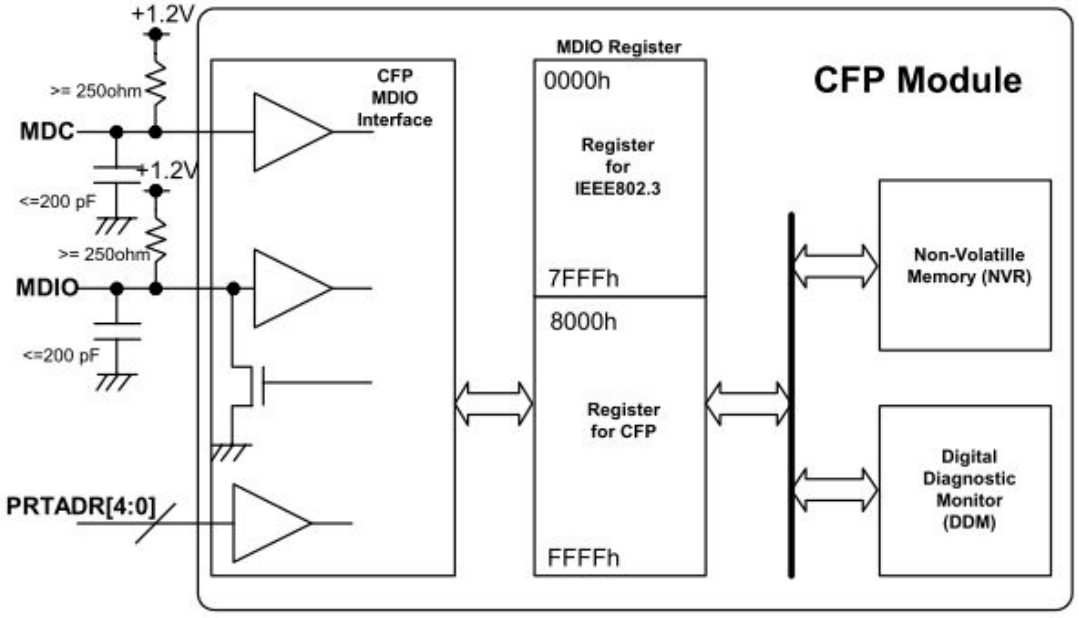


Figure12CFPMDIOInterface

Note:Capacitorrepresents straycapacity600ohmpull-up is preferred

Formoredetailedinformationpleasereferto"***CFPMSAManagementInterfaceSpecificatio nVersion2.2 r06***".

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